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| Feature | Stimulus | Checker List | Priority |
| **Regular** **Write** with **odd** number of data bytes & there are **no coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = odd number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| A dummy data is sent to complete the data word bits | High |
| The slave doesn't abort the write operation | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **Write** with **odd** number of data bytes & there are **coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = odd number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **RETART** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| A dummy data is sent to complete the data word bits | High |
| The slave doesn't abort the write operation | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **Write** with **even** number of data bytes & there are **no coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| The slave doesn't abort the write operation | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **Write** with **even** number of data bytes & there are **coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| The slave doesn't abort the write operation | High |
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| Feature | Stimulus | Checker List | Priority |
| **Regular** **read** with **odd** number of data bytes & there are **no coming** configurations to be executed & allowing short read | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = 1 ;  i\_regf\_wr\_rd\_bit\_tb = 1;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = odd number  i\_rx\_sda\_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| The slave sends all the required data | High |
| A dummy data is sent to complete the data word bits | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **read** with **odd** number of data bytes & there are  **coming** configurations to be executed & allowing short read | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = 1 ;  i\_regf\_wr\_rd\_bit\_tb = 1;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = odd number  i\_rx\_sda\_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **RESTART** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| The slave sends all the required data | High |
| A dummy data is sent to complete the data word bits | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **read** with **even** number of data bytes & there are  **coming** configurations to be executed & allowing short read | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = 1 ;  i\_regf\_wr\_rd\_bit\_tb = 1;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = even number  i\_rx\_sda\_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **RESTART** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave sends all the required data | High |
| The slave sends all the required data | High |

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| Feature | Stimulus | Checker List | Priority |
| **Regular** **read** with **even** number of data bytes & there are **no coming** configurations to be executed & allowing short read | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1 ;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = 1 ;  i\_regf\_wr\_rd\_bit\_tb = 1;  i\_regf\_cmd\_attr\_tb = 0;  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = even number  i\_rx\_sda\_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave sends all the required data | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **one** data byte & there are **coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  i\_regf\_dtt\_tb = xxx;  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **one** data byte & there are **no coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  **i\_regf\_dtt\_tb = 1;**  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **two** data bytes & there are **coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  **i\_regf\_dtt\_tb = 2;**  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern  Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **two** data bytes & there are **no coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  **i\_regf\_dtt\_tb = 2;**  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **three** data bytes & there are **coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 0;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  **i\_regf\_dtt\_tb = 3;**  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |

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| Feature | Stimulus | Checker List | Priority |
| **Immidiate** **Write** with **three** data bytes & there are **no coming** configurations to be executed | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  **i\_regf\_toc\_tb = 1;**  i\_regf\_dev\_index\_tb equals any value except 0;  i\_regf\_short\_read\_tb = x ;  i\_regf\_wr\_rd\_bit\_tb = 0;  **i\_regf\_cmd\_attr\_tb = 1;**  **i\_regf\_dtt\_tb = 3;**  i\_regf\_DATA\_LEN\_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| Flag o\_engine\_done set to 1 after exit pattern | High |
| The slave recognizes its address and pulls down the line to 0 means as an ack | High |
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| Feature | Stimulus | Checker List | Priority |
| The Master in The Reset Mode | i\_sys\_rst\_tb = 1 ;  i\_sys\_rst\_tb = 1->0 ;  i\_sys\_rst\_tb = 0 ;  i\_sys\_rst\_tb = 0->1 ; | @ negedge of i\_sys\_rst\_tb the master enters the rst mode | High |
| o\_scl\_tb line is set to 1 & o\_sdahnd\_serial\_data\_tb is set to 1 (open drain) within time  i\_sys\_rst\_tb is being 0 | High |
| @ posedge of i\_sys\_rst\_tb the master operates normally | High |
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| Feature | Stimulus | Checker List | Priority |
| Enabling N.T Block | i\_sys\_rst\_tb = 1 ;  i\_engine\_en\_tb =1;  i\_engine\_en\_tb =0; | The NT Block doesn't respond until being enabled | High |
| If the enable is high the block excute the required configuration and respond with done | High |

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| Feature | Stimulus | Checker List | Priority |
| **No** **Acknowledgment** for Write or Read operations | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  i\_regf\_wr\_rd\_bit\_tb = 0 or 1;  i\_sda\_rx\_tb = 1 @ the beginning of the first data word | The sequence of sending command word -> Error (no ack) -> RESTART or EXIT depending on the value of (i\_regf\_toc) | High |
| The type of error flag is NACK\_Error | High |

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| Feature | Stimulus | Checker List | Priority |
| **Aborting**  Write operation | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  i\_regf\_wr\_rd\_bit\_tb = 0;  i\_sda\_rx\_tb = 0 @ the beginning of the second or third or fourth or….. data word | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Error(aborting)** -> RESTART or EXIT depending on the value of (i\_regf\_toc) | High |
| The slave aborts the write operation and the type of error flag is BUS\_ABORTED\_Error | High |

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| Feature | Stimulus | Checker List | Priority |
| **Framing Error** | i\_sys\_rst\_tb = 1;  i\_engine\_en\_tb =1;  i\_regf\_wr\_rd\_bit\_tb = 1; | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Error(unexpected bits)** -> RESTART or EXIT depending on the value of (i\_regf\_toc) | High |
| the preamble bits of any word ,crc token values , parity and crc value are not correct | High |
| type of error flag is (CRC\_Error , Parity\_Error |  |